Amendments to the Specification

Please amend the paragraph on page 1, line 24 to page 2, line 9 as follows:

Conventional IC testing is done after all of the layers have been deposited on the wafer. Due to imperfections in the manufacturing process, a certain amount of the ICs will be defective. For instance if the probability of a defect occurring during the deposition of a metallization layer is 1% then the probability of having defective ICs after 7 metallization layers have been deposited is 6.8% which is not insignificant since ICs are mass produced in large quantities. This is an investment on the part of the [[manufactures]] manufacturers that could be mitigated by knowing errors in the manufacturing process before other manufacturing steps are done. Furthermore, because subsequent metallization layers affect the operation of previous metallization layers, it is difficult to ascertain at which point in the manufacturing process the defects occurred. Consequently, IC testing performed before all of the layers have been deposited can provide valuable information that can be used to discover faults in the IC or in the fabrication process. This is especially true for systematic faults such as faulty metal deposition. Test processes that are done before the IC is completed do exist but these tests are done destructively using physical probe contacts or capacitive coupling. Accordingly, none of these testing methods is satisfactory because of their destructive nature.

Please amend the paragraph on page 6, from lines 12-18 as follows:

There may be a plurality of test circuits that are placed on the wafer. The test unit may test each test circuit sequentially or test a plurality of the test circuits in parallel. Each test circuit may be formed adjacent to a die containing the integrated circuit. Alternatively, each test circuit may be formed on a die that contains the integrated circuit. Alternatively, each test circuit may be formed on a large percentage of dies on the wafer. Alternatively, each test circuit may be formed on dies near the edge of the wafer.

Please amend the paragraph on page 15, line 28 to page 16, line 8 as follows:

Referring to Figure 10, the voltage rectifier **52** consists of a network of diodes **D1**, **D2**, **D3**, **D4** and **D5** and capacitors **CVR1**, **CVR2**, **CVR3**, **CVR4** and **CVR5**. The antenna **50** is connected at node **A1**. The diode **D1**, which is connected to node **A1**, and the capacitor **CVR1** rectify the incoming RF power signal **32** to provide a DC voltage **VUR1** which is an unregulated voltage. The voltage **VUR1**, in combination with the capacitors **CVR2** and **CVR3** and the diodes **D2** and **D3** creates a doubled voltage **VUR2**. This process is repeated using the voltage **VUR3**, the diodes **D4** and **D5** and the capacitors **CVR4** and **CVR5** to produce a tripled voltage **VUR3**. The voltages **VUR1**, **VUR2** and **VUR3** are used for power by the other parts of the test circuit **14**. In the present design the diodes are constructed out of N-well FETs that are connected as diodes as is commonly known to those skilled in the art. Alternatively, Schottky diodes may be used.

Please amend the paragraph on page 16, line 28 to page 17, line 6 as follows:

Reference is now made to Figure 12 which shows that the ring oscillator **58** consists of five [[invertors]] inverters **I1**, **I2**, **I3**, **I4** and **I5**, which are connected in a series loop feedback configuration. The ring oscillator **58** is adapted to provide a clock signal **90** that is used to synchronize the test circuit **14**. The clock signal **90** may be at a frequency which is comparable to the frequency at which the IC **18** was designed to operate which may, for example, be in the range of several hundred MHz to several GHz. During each half period of the clock signal **90**, the signal will propagate around the loop with an inversion. If each inverter (**I1**, **I2**, **I3**, **I4** and **I5**) have similar loads at their output nodes then each inverter has a similar delay (τ_{inv}) so that a half period of the clock signal **90** is $n*\tau_{inv}$ seconds long. The clock signal **90** therefore has a frequency of $1/(2*n*\tau_{inv})$ Hz.

Please amend the paragraph on page 17, from lines 7-17 as follows:

Ring oscillators are standard in IC design, however, it is typical to use a ring oscillator which consists of a large odd number of [[invertors]] inverters such as 101

inverters. A large number of inverters is required because in probe testing, sub-nanosecond test signals [[can not]]cannot be propagated. However, since RF signals are used in the wireless IC test system **10** of the present invention, the clock signal **90** may have a higher frequency that can be used in the test circuit **14**. Accordingly, the ring oscillator **58** may consist of a substantially lower number of inverters. Furthermore, a crucial design constraint for the ring oscillator **58**, as well as the other circuitry in the test circuit **14**, is that the ring oscillator **58** operates over a wide range of supply voltage levels and IC technologies.

Please amend the paragraph on page 18, from lines 7-14 as follows:

Referring now to Figure 15, the sequencer **60** comprises nine D flip-flops **110**, **112**, **114**, **116**, **118**, **120**, **122**, **124** and [[**124**]]**126** connected in series in a shift register format and two inverters **I6** and **I7**. The number of D flip-flops correlates with the number of test states which will be described in greater detail below. As such, the number of D flip-flops may vary depending on the number of test states that are used in the test circuit **14**. The sequencer **60** was also designed using dynamic logic D flip-flops for the reasons previously stated for the divider **59**.

Please amend the paragraph on page 18, from lines 15-33 as follows:

The sequencer **60** shifts one bit through the chain of D flip-flops upon each transition of the reduced clock signal [[**96**]] **104** from a digital logic value of '0' to a digital logic value of '1' (a negative edge triggered flip-flop may also be used). The output **S9** of the final D flip-flop **126** is recycled to the input **128** of the first D flip-flop **110**. The sequencer **60** provides test enable signals (i.e. state signals **S2**, **S3**, **S4**, **S5**, **S6**, **S7**, **S8** and **S9**). The sequencer **60** ensures that only one state signal has a digital logic value of '1' for a given period of the clock signal **90**. Once the state signal **S9** has a digital logic value of '1', the state signal **S9** is used to reset each of the D flip-flops in the sequencer **60**. The state signal **S9** also creates a digital logic value of '1' at the input **128** of the first flip-flop **110** to restart the sequence of test enable signals. This particular implementation was chosen for its minimal transistor count and the ability to operate

with very low supply voltages. However, dynamic power consumption is not as critical for the sequencer **60** since the sequencer **60** is operated at 1/32 of the clock signal **90**. Additional circuitry for master reset and startup functionality (i.e. inverters **I6** and **I7**) are included so that a new test can be started as fast as possible after power up of the test circuit **14**. The two inverters **I6** and **I7** ensure that there is a good square edge or hard transition for the input signal **128** to the first D flip-flop **110**.

Please amend the paragraph on page 20, from lines 1-8 as follows:

To accomplish parameter testing, one embodiment switches the sub-circuits into and out of the variable ring oscillator **62** based on the test state signals **S1**, **S2**, **S3**, **S4**, **S5**, **S6**, **S7**, **S8** and **S9** which are supplied by the sequencer **60**. Most of the sub-circuits that are switched into the variable ring oscillator **62** load the variable ring oscillator such that the sub-circuit will affect the frequency of oscillation of the variable ring oscillator **62**. Differences in the frequency of oscillation of the variable ring oscillator **62** will then allow for parameter measurement as will be shown below.

Please amend the paragraph on page 24, from lines 8-19 as follows:

Referring to Figure 20, during test state 1, the state signals **NS2**, **NS3** and **NS6** have a digital logic value of '1'. Accordingly, the components of the variable ring oscillator **62** which are enabled during test state 1 are the transmission gates **TN2**, **TN3** and **TN6** and the sub-circuit **152** which comprises inverters **I17** and **I18**. The sub-circuit **152** is connected to the base ring oscillator **150** such that the variable ring oscillator **62** now comprises five inverters. Accordingly the frequency of oscillation for the variable ring oscillator **62** is $1/(2*5*\tau_{inv})$ Hz where τ_{inv} is the delay for each inverter **I11**, **I12**, **I13**, **I14** and **I15** assuming that each inverter has similar parasitic capacitive loads. The frequency of oscillation for the variable ring oscillator **62** could be measured in this test state and used along with test state 6 to measure the parameter of gate delay.

Please amend the paragraph on page 26, from lines 5-19 as follows:

Reference is next made to Figure 23 which shows the elements of the variable ring oscillator **62** that are enabled during test state 4 in which the state signals **S4, NS2, NS3** and **NS6** have a digital logic value of '1'. In this case, the transmission gates **TN2, TN3** and **TN6**, and the transistor **QA** are enabled so that the sub-circuits **152** and **158** are connected to the base ring oscillator **150**. Therefore, the variable ring oscillator **62** comprises five inverters **I11, I12, I13, I17** and **I18** and has a load consisting of a resistor **R1** in series with a capacitor **C3**. The impedance of this load is chosen such that it is much larger than the parasitic loads of each inverter **I11, I12, I13, I21** and **I22** in the variable ring oscillator **62**. The delay of the variable ring oscillator **62** is thus determined by the serial combination of the resistor **R1** and the capacitor **C3**. The frequency of operation of the variable ring oscillator **62** is $1/(k*R1*C3)$ Hz (following the guidelines outlined for Figure 17a and replacing R_{lump} with R1). Therefore the frequency of oscillation is proportional to the resistance of the resistor **R1**.

Please amend the paragraph on page 32, from lines 4-13 as follows:

A spectrum of test results is shown in Figures 30a and 30b. Referring to Figure 30a, for capacitance, there was a distinct difference between the two frequencies exhibited (labeled **c1** and **c2**) by the test circuit **14** when the variable ring oscillator **62** was loaded first by sub-circuit **154** and then by sub-circuit **156**. The resistance parameter test results also showed distinct oscillation frequencies (the frequencies are labeled **r1** and **r2**). Figure 30b shows the simulation results for the gate delay parameter test[[,]]. In this case, there was also two discernible oscillation frequencies **d1** and **d2**. The extra delay, and hence lower oscillation frequency, due to the two extra inverters is labeled **d2**.

Please amend the paragraph on page 33, from lines 4-11 as follows:

One implementation of the test circuit **14** was done for exemplary purposes, with standard [[VLSI]] VLSI CAD tools, using a 5 layer 0.25 micron, 2.5 V, single n-well CMOS process. The final layout, without the antenna, was approximately 150 by 50 micrometers and comprised approximately 250 transistors. This results in a chip area of 7,500 μm^2 which is approximately $1/10{,}000^{th}$ the area of a Pentium class IC. The test circuit **14** dissipates approximately 1 mW of power which is $1/20{,}000^{th}$ of the power dissipation of a Pentium class IC.